Multilevel Inverter: A Review on Methodology, Topologies & Techniques

(IJCSNT) International Journal of Communication Systems and Network Technologies
ISSN Number: 2053-6283
Volume 6, Issue No. 1, 8–18

https://journals.mirlabs.in/index.php/ijcsnt
DOI-10.18486/ijcsnt/6.1.076
IJCSNT

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Abstract

In Power-Electronic Systems, Multi-Level Inverters are growing as new topologies which propose options for high voltage and medium voltage. From different levels of DC voltage source, a Multi-Level Inverter (MLI) generates the characteristic staircase voltage wave, where this DC voltage source comes from various renewable energy sources like fuel cell, solar cell, etc. Because of the gate driver circuit, the complexity of the system is higher which results in the major drawback of the Multi-Level Inverter. This paper discusses the Multi-Level Inverter methodology and various topologies like (1) Diode-clamped, (2) Flying-capacitor and (3) Cascaded Multi-Level Inverters with separate DC sources. Various types of switching schemes used in Multi-Level Inverter topologies like the Pulse Width Modulation (PWM) scheme have also been discussed in this paper.

Keywords

Multi-level Inverters, MLI, Asymmetric and Symmetric Voltage Source Configuration, Hybrid Topologies, CHB, THD, Phase Opposition Disposition, Sinusoidal Pulse Width Modulation, PWM, Phase Shift Pulse Width Modulation

Received: 21 December 2016; **Revised:** 31 March 2017; **Accepted:** 27 April 2017;
Published: 30 April 2017;

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Introduction

Beginning of use inverter topologies, there is only two level of inverter that has two level voltages +V and –V, these two level of voltage switched from Pulse width modulation (PWM) technique and this methodology create efficacious harmonics distortion, EMI and dv/dt stress. The main problem of total harmonic distortion (THD), higher ratio present in wave form, and it is tough to connect directly higher power and medium voltages (i.e. 2.3, 3.3, 4.16, or 6.9 kV) to power electronics devices[1]. For this new multilevel inverter (MLI) topology invented, these topologies help with working advanced voltage levels. Multi-level inverters (MLI) have shown more consideration in industrial application, such as renewable energy systems, static VAR compensators (DSTATCOM, DVR), and motor driver, etc. as result the inverter output voltages have high quality of sinusoidal waveform and improved harmonic distortions[1] [2]. A number of multi-level inverter (MLI) topologies have been invented during the last decades, diode clamped (neutral l clamped), cascaded H-bridges inverter (CHB) with separate dc sources, and flying capacitors (capacitors clamped) are three major used multi-level inverter methodologies.

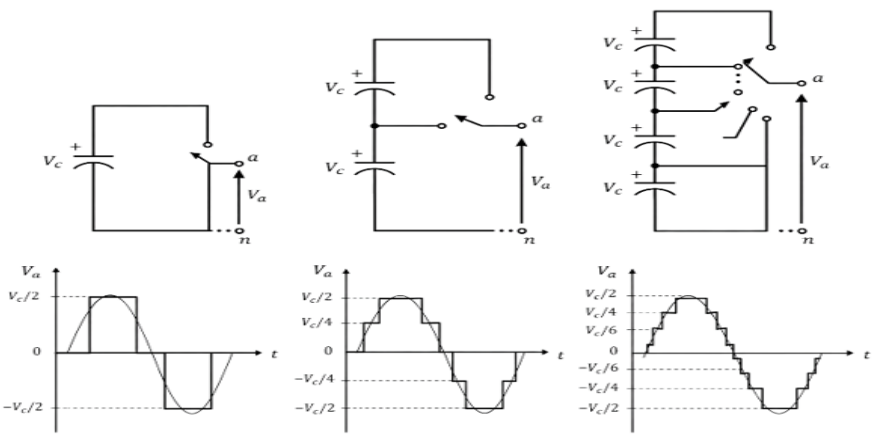

Figure 1. Single phase of an inverter with (a) 2 levels, (b) 3 levels, and (c) n levels.

Multi-level inverter includes number of ideal power electronics switch; capacitors and flying diodes are connected to received higher number of stepped waveform, the term introduced multi-level starts with the 3-level inverter. In the inverter, by growing the number of stepped levels, the output voltages have more levels producing a staircase waveform, which consists of a reduced THD (total harmonic distortion). However, an increased number of voltage levels increases the control complexity and presents voltage imbalance problems. There are some different topologies which have been introduced for this higher number of levels decreases the voltage stress on the power electronics devices, and improve total harmonic profile.

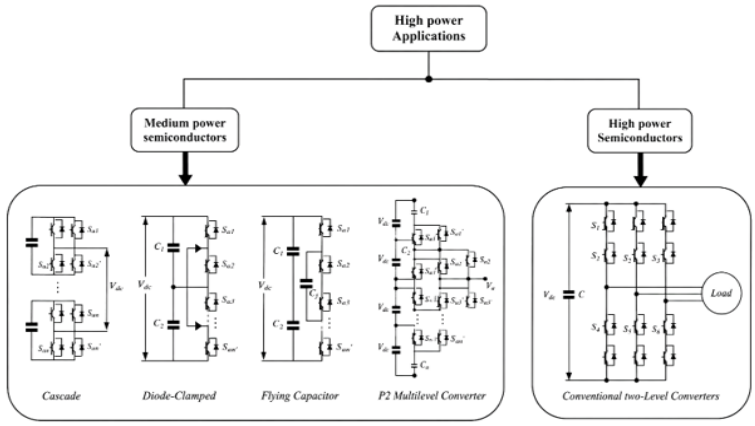

Figure 2. PWM techniques (phase shifted and level shifted).

Multi Level Inverter Methods

Diode-Clamp Multilevel Converter

In Diode Clamp MLI topology, split of the dc-bus voltage into required levels by diodes and bulk capacitors connected in series. The neutral point is described as the middle point of the capacitors. The voltage at output has 5 voltage levels:

1. $V_{dc}/2$
2. $V_{dc}/4$
3. 0
4. $-V_{dc}/2$
5. $-V_{dc}/4$

Switches S_1, S_2, S_3, and S_4 needs to be turned ON for voltage level $V_{dc}/2$ and for $-V_{dc}/2$ switch for S_1', S_2', S_3', S_4' need to be turned ON. $V_{dc}/4$ is the voltage across each capacitor and through clamping diodes, voltage stress of each device will be restricted to single capacitor voltage level $V_{dc}/4$[3,4].

To describe how the staircase voltage is process, the Neutral point (N) is measured as the reference point of output phase voltage. To process 5-level voltages across a and n, there are few switch combinations which are explained & shown in table below: Switch stats for 5-level Capacitor-clamped inverter, “1” stands for Turned ON and “0” stands for Turned OFF switches

Advantages:

1. THD (Total Harmonic Distortion) elements will be low enough to lessen the filters use, only when the number of voltage levels is high enough.
2. Since all the working devices are switched at the basic fundamental frequency, hence working efficiency is high.
3. For a back-to-back system, the control method is simple.

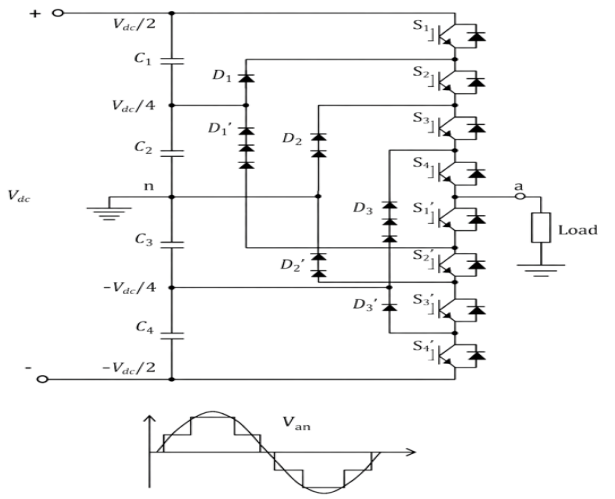

Figure 3. Diode-clamped MLI circuit topology of 5-level.

Table 1. Switching States for Different Output Voltage Levels

Output Voltage	$\mathbf{S_1}$	$\mathbf{S_2}$	$\mathbf{S_3}$	$\mathbf{S_4}$	$\mathbf{S_1'}$	$\mathbf{S_2'}$	$\mathbf{S_3'}$	$\mathbf{S_4'}$
$V_{dc}/2$	1	1	1	1	0	0	0	0
$V_{dc}/4$	0	1	1	1	1	0	0	0
0	0	0	1	1	1	1	0	0
$-V_{dc}/2$	0	0	0	1	1	1	1	0
$-V_{dc}/4$	0	0	0	0	1	1	1	1

4. By this technique, Reactive power flow can be controlled.

Disadvantages:

1. When the number of levels is high, a higher number of clamping diodes is required.
2. Real power flow control is difficult to do for the Diode-Clamped MLI[5,6].

Multilevel Converter Using Flying-Capacitor

The voltage process in 5-level capacitors-clamped topology is more flexible and is efficient than the diode-clamped converter as shown in Figure **??**. The voltage of the 5-level phase-leg output with respect to N (the neutral point), 5-level voltage can be processed by the following voltage combinations:

$$\frac{V_{dc}}{2},\ \frac{V_{dc}}{4},\ 0,\ -\frac{V_{dc}}{2},\ -\frac{V_{dc}}{4}.$$

Switches S_1, S_2, S_3, and S_4 needs to be turned ON for voltage level $\frac{V_{dc}}{2}$ and for $-\frac{V_{dc}}{2}$ switch for S_1', S_2', S_3', and S_4' need to be turned ON[7].

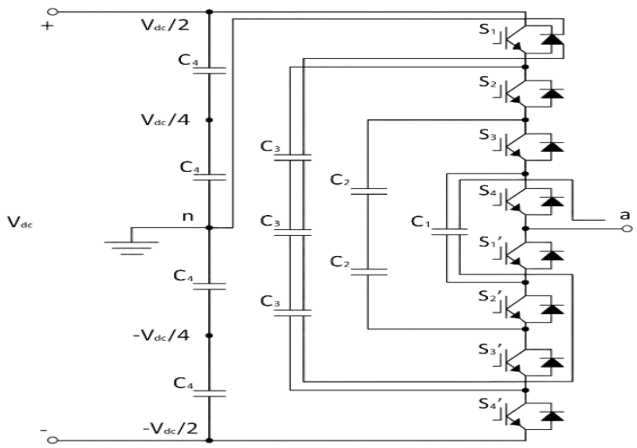

Figure 4. Capacitor-clamped MLI circuit topology of 5-level.

Shown in figure using fundamental building block of capacitor clamp, the circuit has been known as the flying capacitor multilevel inverter[6]. The inverter in shown in figure produce five voltage level which as shown in figure[8,9]. Switch stats for five level capacitor clamped inverter, "1" means turned on and "0" means turn off switches

Table 2. Switching States for Different Output Voltage Levels

Output Voltage	$\mathbf{S_1}$	$\mathbf{S_2}$	$\mathbf{S_3}$	$\mathbf{S_4}$	$\mathbf{S_1'}$	$\mathbf{S_2'}$	$\mathbf{S_3'}$	$\mathbf{S_4'}$
$\mathbf{V_{dc}/2}$	1	1	1	1	0	0	0	0
$\mathbf{V_{dc}/4}$	1	1	1	0	1	0	0	0
$\mathbf{0}$	1	1	0	0	1	1	0	0
$\mathbf{-V_{dc}/2}$	1	0	0	0	1	1	1	0
$\mathbf{-V_{dc}/4}$	0	0	0	0	1	1	1	1

In the preceding description, the capacitors which are in discharging mode are denoted by positive signs $(+v)$, while those in charging mode are denoted by negative sign $(-v)$. By suitable selection of capacitor combinations, balancing the capacitor charge becomes possible. Analogous to diode clamping, a good number of bulk capacitors are required by capacitor clamping. Note that each capacitor's voltage rating used is similar to that of the main power electronic devices[8].

Advantages:

1. During power outage, a good number of storage capacitors deliver extra capability.
2. To balance different voltage levels, it provides power electronics switch combination redundancy.

3. In case the number of levels is higher, the total harmonic content will be sufficient to avoid the use of filters.
4. By making a possible VSI (Voltage Source Inverter) candidate for high voltage transmission, both real power and reactive power flow could be controlled.

Disadvantages:

1. Higher no. of storage capacitors is projected when the no. of inverter voltage levels is high. For expensive and bulky capacitors, High-voltage level converter is much expensive and is more difficult to package.
2. The MLI control will be very complex, and the switching losses and switching frequency will be high for real power transmission [5].

Multi-Level Converter Using Cascaded-Inverters with Separate DC Source

Cascaded- multilevel inverters with separate dc voltage source efficient to use in comparison to the other two topologies as there is no need of extra elements as capacitor and diode to clamping and there are used different asymmetric voltage source inverter(VSI) from renewal energy source as fuel cell, solar cell wind energy etc [2]. Higher of no. of voltage level could be achieved by adding inverter cell, and produce smooth sine wave and lower THD ratio [1]. One of major disadvantage is higher number of power electronics switches use for controlling this power switch use gate driver circuit due to this circuit is some place is complex [9,10].

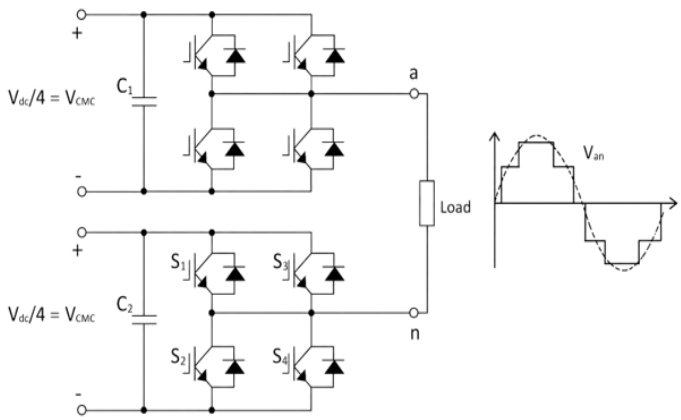

Figure 5. Cascaded Multi-level Inverters with separate dc source.

Advantages:

1. To get the same number of voltage levels, it needs the least number of components among all multilevel converters.
2. Voltage balancing capacitors or clamping diodes are not required.

3. In this structure, soft-switching could be used so as to avoid bulky and lossy resistor-capacitor-diode snubber circuits.

Disadvantage:

1. Separate dc voltage sources are required for real power conversions, and hence its applications are sometimes limited [2].

Switching Scheme

The switching scheme is divided in to two methods and for both cases stepped output wave form is achieved.

1. High switching scheme
2. Fundamental switching scheme

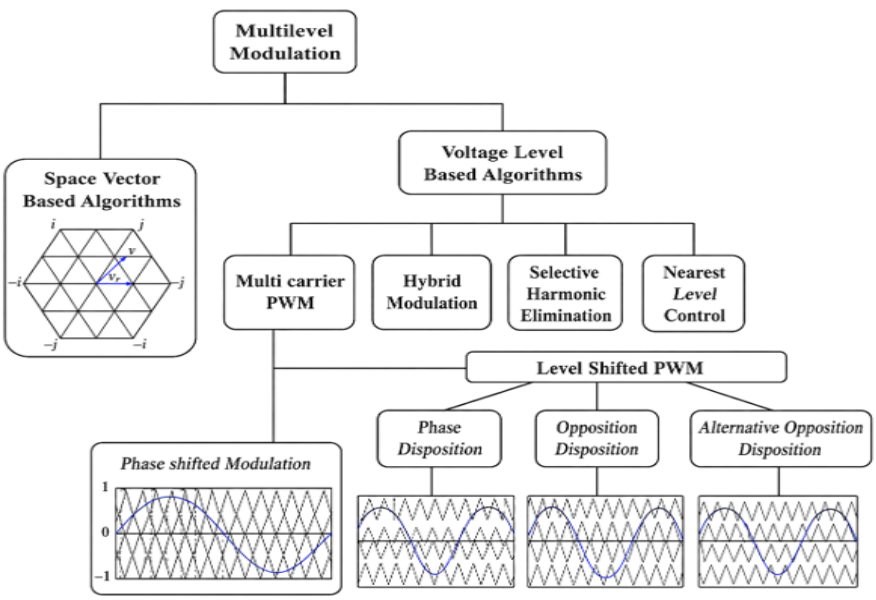

Figure 6. Details of phase shifted and level shifted PWM techniques (top to bottom).

Different PWM Techniques

Multi-level Inverter methods use high frequency carrier waves (triangular wave) in comparison to reference wave (Sinusoidal) that produce switch gate pulses, and this modulation technique helps to reduce the Total Harmonics Distortion (THD) profile [4].

There different PWM techniques are:

1. Phase disposition (PD)
2. Phase opposite Disposition (POD)
3. Alternation Phase Disposition (APOD)
4. Phase shift (PS)

These techniques are shown in below figures: -

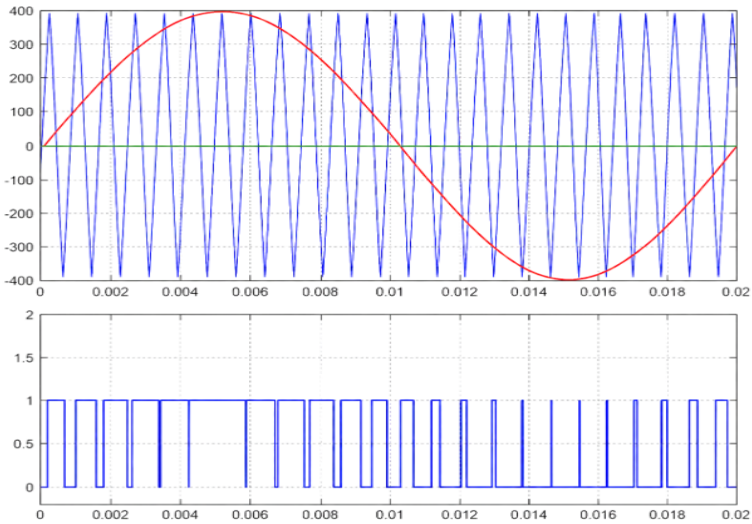

Figure 7. PWM carrier triangular and reference sinusoidal wave and pulses.

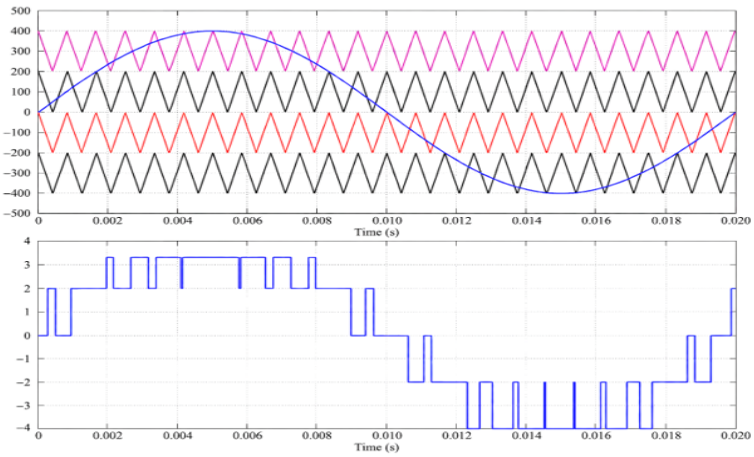

Figure 8. PDPWM carrier triangular and reference sinusoidal wave and pulse.

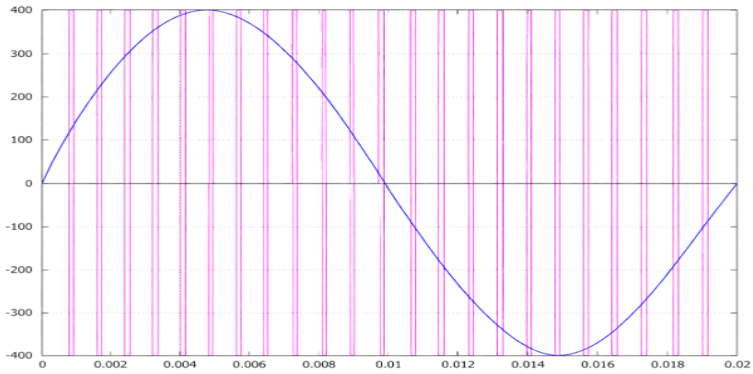

Figure 9. Phase Shift (PS).

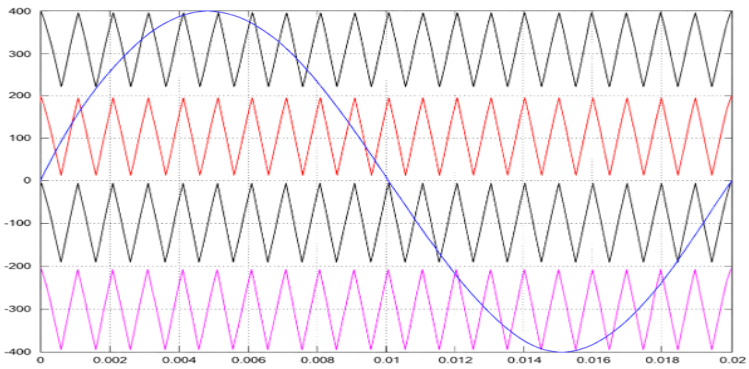

Figure 10. Alternate Phase Opposite Disposition (APOD).

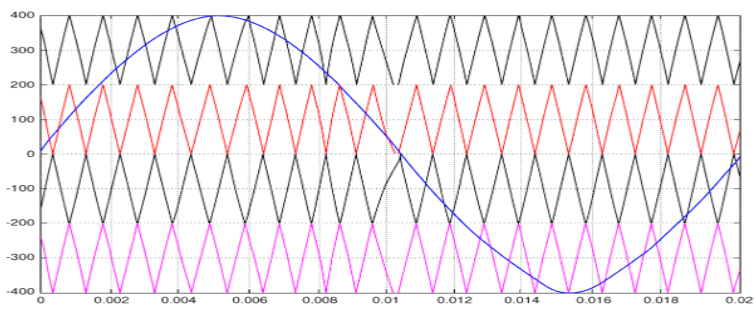

Figure 11. Phase Opposite Disposition (POD).

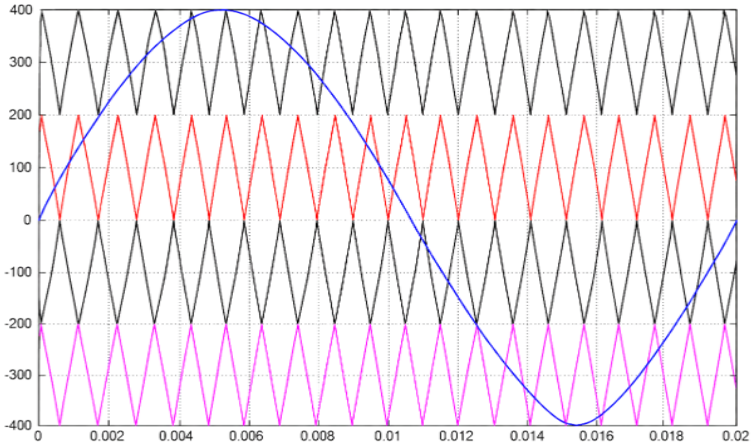

Figure 12. Phase Disposition (PD).

Applications:

A. Back-to-Back Intertie
B. Reactive Power Compensation
C. Utility Compatible Regulating Speed Drives

Table 3. Comparison of Different Multilevel Inverter Configurations

Inverter Configuration	**Diode-Clamp**	**Flying-Capacitors**	**Cascaded Inverters**
Switching devices	$2(m-1)$	$2(m-1)$	$2(m-1)$
Main diodes	$2(m-1)$	$2(m-1)$	$2(m-1)$
Clamping diodes	$(m-1)(m-1)$	0	0
DC bus capacitors	$(m-1)$	$(m-1)$	$\frac{(m-1)}{2}$
Balancing capacitors	0	$\frac{(m-1)(m-2)}{2}$	0

Conclusion

The multi-level inverters have emerged from analytical thought to real applications due to numerous outstanding advantages like the opportunity of linking directly to high power quality, medium voltage, high availability, high degree of modularity, both output and input, and the control of flow of power in the reincarnate version. These topologies of cascaded multi-level inverters (MLI) based on application are presented. This paper has discussed the applications and recent developments of these newly proposed topologies, modulation, techniques, and control strategies of Multi-Level Inverters.

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